

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S33	12	S32 and (clock near10 data near10 ((in near2 phase) (out near4 phase)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 13:46
S32	190	S29 and ((DDR or double adj data adj rate) and (clock near10 data same (phase sync\$11)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 13:45
S31	206	S29 and ((DDR or double adj data adj rate) and (clock same data same (phase sync\$11)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 13:35
S18	1	(DDR or double adj data adj rate) and AC near4 loopback	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 13:33
S30	3	S29 and (AC adj I/O adj loopback)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 12:40
S29	19161	(714/30,700,718,721,724,738,744, 811,814,815,817,819 713/400 326/38,63,86,96 371/22.1,22.5 365/200,201).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 12:39
S19	12478	(714/30,700,718,721,724,738,744, 811,814,815,817,819 713/400 326/38,63,86,96 371/22.1,22.5). ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 12:39
S2	3	AC adj I/O adj loopback	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 12:39
S28	15	US-6019639-\$.DID. OR US-6218910-\$.DID. OR US-6501343-\$.DID. OR US-6622103-\$.DID. OR US-5748006-\$.DID. OR US-6236572-\$.DID. OR US-6587896-\$.DID. or 20030006856-\$.DID. or "20020175697" or 20020074653-\$. DID. or 20010034865-\$.DID.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 12:36

S27	2	("6671787").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 12:35
S1	6	("5621739" "6005412" "6031385").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/14 11:21
S26	4	("6574758" "5349587").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/12 09:31
S25	37	S24 and (("double data rate" DDR) same (buffer I/O))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 15:03
S24	93	("double data rate" DDR) same (test\$3 near3 (pattern signal data)) and (clock near4 generat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 15:02
S23	1	("double data rate" DDR) same (memory near2 controller) same (test\$3 near3 (pattern signal data) near2 generat\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 14:59
S20	79	("double data rate" DDR) same (memory near2 controller) same ((pattern signal data) near2 generat\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 14:41
S22	65	S20 and (clock near5 control\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 14:34
S21	65	S20 and clock near5 control\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 14:33
S11	6	(double adj data adj rate near4 test\$3) and memory near2 controller and (pattern near2 generat\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 14:29

S5	48	double adj data adj rate near4 test\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/29 15:57
S3	14299	DDR or double adj data adj rate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/28 13:23
S17	2	((("5621739" "6005412" "6031385"). pn.) and phase	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/27 15:49
S16	2	((US-6647521-\$ or US-6556492-\$ or US-6658604-\$ or US-6629274-\$ or US-6477674-\$).did. or (US-20030120989-\$ or US-20030101376-\$ or US-20020012283-\$ or US-20030005374-\$).did.) and PLL	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/27 15:33
S15	9	(US-6647521-\$ or US-6556492-\$ or US-6658604-\$ or US-6629274-\$ or US-6477674-\$).did. or (US-20030120989-\$ or US-20030101376-\$ or US-20020012283-\$ or US-20030005374-\$).did.	US-PGPUB; USPAT	OR	OFF	2004/04/27 15:33
S14	1	"5905391".PN.	US-PGPUB; USPAT	OR	ON	2004/04/27 15:14
S13	1	"6239642".PN.	US-PGPUB; USPAT	OR	ON	2004/04/27 15:14
S12	15	AC near4 loopback	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/27 15:09
S10	2	(double adj data adj rate near4 test\$3) and memory adj controller and (pattern near2 generat\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/27 15:05
S6	12	(double adj data adj rate near4 test\$3) and buffer and (pattern near2 generat\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/27 15:03
S9	1	"6311300".PN.	US-PGPUB; USPAT	OR	ON	2004/04/27 14:47

S8	1	"6415403".PN.	US-PGPUB; USPAT	OR	ON	2004/04/27 14:47
S7	1	"6467054".PN.	US-PGPUB; USPAT	OR	ON	2004/04/27 14:46
S4	3014	double adj data adj rate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/27 14:29



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... Similar approach of using two-XOR logic gates **in phase** ... recovered **clock rate** can be one half of the **data rate**. Thus, ...

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... When PWRDWN\ is high, the outputs switch **in phase** and frequency with CLK. ...

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... along with the **data**. Since the transmit **clock** remains **in phase** with the **data**

... **DDR (double data rate)** technique which allows **clock** and **data** lines to ...

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**PLLs in Cyclone Devices**

... there is a stable **clock** output signal **in phase** with the reference **clock**. ...

feature is useful in **double data rate (DDR)** applications where the **data** is ...

[www.altera.com/products/devices/cyclone/features/cyc-pll\\_features.html](http://www.altera.com/products/devices/cyclone/features/cyc-pll_features.html) - [Cached](#) - [Similar pages](#)

**External Memory Interfaces in Cyclone II Devices**

... of the **clock**, **DDR SDRAM** devices effectively **double** total **data** bandwidth ...

is sent to the memory device on both edges of the **in-phase** system **clock**, ...

[www.altera.com/products/devices/cyclone2/features/cy2-ext\\_mem\\_int.html](http://www.altera.com/products/devices/cyclone2/features/cy2-ext_mem_int.html) - [Cached](#) - [Similar pages](#)

**[PDF] Design Optimization Techniques for Double Data Rate SDRAM Modules**

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... signals are **double data rate** and transfer on both edges of the **clock** signals,

... On **DDR DIMMs**, the **clock** to the register should be **in phase** with the ...

[www.fl-eng.com/specs/fairchild\\_ddr.pdf](http://www.fl-eng.com/specs/fairchild_ddr.pdf) - [Similar pages](#)

**Easy DDR Memory Interface Design in Low-Cost FPGAs**

... Systems designers are using economical **double data rate (DDR)** memory in a ...

which could occur **in phase** with either a positive or negative **clock** edge. ...

[www.nsdnewsletter.com/English/Newsletters/2004/Articles/200412\\_Article\\_EasyDDR.html](http://www.nsdnewsletter.com/English/Newsletters/2004/Articles/200412_Article_EasyDDR.html) - [Cached](#) - [Similar pages](#)

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... FIFOs will therefore run at 160MHz **clock rate**. **Data** transfer on the TPM will

also take place ... 320Mbit/s **DDR in phase** with the local board **clock**. ...

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